

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Canceled)

Claim 2 (New): An apparatus for exercising semiconductor devices, said apparatus comprising:

 a plurality of semiconductor devices, each comprising a plurality of elongate, spring connection elements;

 a support substrate comprising a plurality of terminals;

 test connection means for connecting said terminals to a test device;

 a plurality of socket substrates disposed on said support substrate, each said socket comprising a plurality of sockets and a plurality of traces, each said trace electrically connected to one of said sockets;

 means for electrically connecting ones of said traces with ones of said terminals; and

 means for pressing ones of said spring connection elements against ones of said sockets, wherein said spring connection elements generate spring counterforces and thereby form pressure connections with said sockets.

Claim 3 (New): The apparatus of claim 2, wherein said plurality of semiconductor devices are dies of an unsingulated semiconductor wafer.

Claim 4 (New): The apparatus of claim 3, wherein each socket substrate corresponds to one die.

Claim 5 (New): The apparatus of claim 3, wherein said support substrate is part of a probe card assembly.

Claim 6 (New): The apparatus of claim 5, wherein said support substrate is electrically connected through an interposer to a probe card, and wherein said support substrate, said interposer, and said probe card compose said probe card assembly.

Claim 7 (New): The apparatus of claim 2, wherein said semiconductor devices are unpackaged, singulated semiconductor dies.

Claim 8 (New): The apparatus of claim 2, wherein said test device provides test signals to test a functionality of said semiconductor devices.

Claim 9 (New): The apparatus of claim 2, wherein said test device provides power to said semiconductor devices, and further comprising a temperature control device disposed to control a temperature of said semiconductor devices.

Claim 10 (New): The apparatus of claim 9, wherein said temperature control device comprises:
a first thermal chuck in thermal contact with said semiconductor devices; and
a second thermal chuck in thermal connect with said socket substrates.

Claim 11 (New): The apparatus of claim 2, wherein said socket substrates are disposed in rows on said support substrate, and further comprising a plurality of power lines disposed on said support substrate, each said power line corresponding to one of said rows of socket substrates and supplying power to every socket substrate in said row.

Claim 12 (New): The apparatus of claim 11, further comprising a plurality of isolation resistors, each said isolation resistor disposed between one of said power lines and one of said socket substrates.

Claim 13 (New): The apparatus of claim 2, wherein said means for securing comprises one of a test head or a vacuum chuck.

Claim 14 (New): The apparatus of claim 2, wherein said means for electrically connecting ones of said traces with ones of said terminals comprise a plurality of bond wires, each said bond wire bonded to one of said traces and to one of said terminals.

Claim 15 (New): The apparatus of claim 2, wherein said sockets comprise pits etched into a surface of a corresponding socket substrate.

Claim 16 (New): The apparatus of claim 2, wherein said socket substrate comprises silicon.

Claim 17 (New): A test socket apparatus comprising:

 a support substrate comprising a plurality of terminals;
 test connection means for connecting said terminals to a test device;
 a socket substrate disposed on said support substrate and comprising a plurality of sockets and a plurality of traces, each said trace electrically connected to one of said sockets;
 means for electrically connecting ones of said traces with ones of said terminals; and
 means for pressing elongate spring connection elements disposed on said semiconductor device against said sockets such that said spring connection elements generate spring counterforces and thereby form pressure connections with said sockets.

Claim 18 (New): The apparatus of claim 17, wherein said test device provides test signals to test a functionality of said semiconductor device.

Claim 19 (New): The apparatus of claim 17, wherein said test device provides power to said semiconductor device, and further comprising thermal means for controlling a temperature of said semiconductor device.

Claim 20 (New): The apparatus of claim 17, wherein said means for electrically connecting ones of said traces with ones of said terminals comprise a plurality of bond wires, each said bond wire bonded to one of said traces and to one of said terminals.

Claim 21 (New): The apparatus of claim 17, wherein said sockets comprise pits etched into a surface of said socket substrate.

Claim 22 (New): The apparatus of claim 17, wherein said socket substrate comprises silicon.

Claim 23 (New): The apparatus of claim 17 further comprising a plurality of said socket substrates.

Claim 24 (New): A method of making a test socket apparatus, said method comprising:
providing a support substrate comprising a plurality of terminals;
disposing a socket substrate on said support substrate, said socket substrate comprising a plurality of sockets, each said socket configured to receive an elongate spring connection element of a semiconductor device, said socket substrate further comprising a plurality of traces, each said trace electrically connected to one of said sockets;
electrically connecting ones of said traces with ones of said terminals.

Claim 25 (New): The method of claim 24 further comprising disposing a plurality of said socket substrates on said support substrate.

Claim 26 (New): The method of claim 25, wherein said step of disposing a plurality of said socket substrates further comprises disposing said socket substrates to correspond to a plurality of said semiconductor devices.

Claim 27 (New): The method of claim 26, wherein said semiconductor devices are dies of an unsingulated semiconductor wafer.

Claim 28 (New): The method of claim 27, wherein each one of said socket substrates corresponds to one of said semiconductor dies.

Claim 29 (New): The method of claim 25 further comprising securing said support substrate to a probe card assembly.

Claim 30 (New): The method of claim 25 further comprising:

providing a first temperature control device disposed to make thermal contact with said semiconductor devices; and

providing a second temperature control device disposed to make thermal contact with said socket substrates.

Claim 31 (New): The method of claim 25 further comprising:

disposing said plurality of socket substrates in rows on said support substrate, and

providing a plurality of power lines, each said power line corresponding to one of said rows of socket substrates and supplying power to every socket substrate in said row.

Claim 32 (New): The method of claim 31 further comprising providing a plurality of isolation resistors, each said isolation resistor disposed between one of said power lines and one of said socket substrates.

Claim 33 (New): The method of claim 24, wherein said step of electrically connecting ones of said traces with ones of said terminals comprises:

bonding a bond wire to one of said traces; and

bonding said bond wire to one of said terminals.

Claim 34 (New): The method of claim 24, wherein said sockets comprise pits etched into a surface of a corresponding socket substrate.

Claim 35 (New): The method of claim 24, wherein said socket substrate comprises silicon.

Claim 36 (New): The method of claim 24 further comprising providing a temperature control device for controlling a temperature of said semiconductor device.